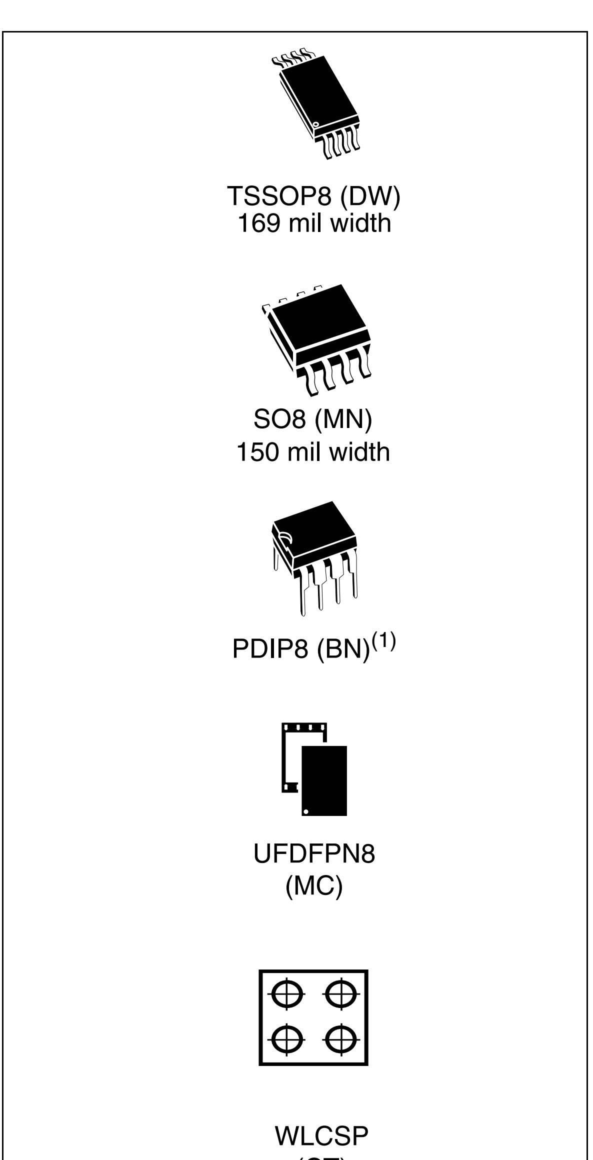


M24C08-W M24C08-R M24C08-F

8-Kbit serial I²C bus EEPROM

Datasheet- production data



1. Not recommended for new designs

Features

- Compatible with all I²C bus modes:
  - 400 kHz
  - 100 kHz
- Memory array:
  - 8 Kbit (1 Kbyte) of EEPROM
  - Page size: 16 bytes
- Single supply voltage:
  - M24C08-W: 2.5 V to 5.5 V
  - M24C08-R: 1.8 V to 5.5 V
  - M24C08-F: 1.7 V to 5.5 V (full temperature range)
    and 1.6 V to1.7 V (limited temperature range)
- Write:
  - Byte Write within 5 ms
  - Page Write within 5 ms
- Operating temperature range: from -40 °C up to +85 °C
- Random and sequential Read modes
- Write protect of the whole memory array
- Enhanced ESD/Latch-Up protection
- More than 4 million Write cycles
- More than 200-year data retention

Packages

- PDIP8 ECOPACK1®
- SO8 ECOPACK2®
- TSSOP8 ECOPACK2®
- UFDFPN8 ECOPACK2®
- WLCSP ECOPACK2®

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1 Description

The M24C08 is an 8-Kbit I^2C-compatible EEPROM (Electrically Erasable PROgrammable Memory) organized as 1 K × 8 bits.

The M24C08-W can be accessed with a supply voltage from 2.5 V to 5.5 V, the M24C08-R can be accessed with a supply voltage from 1.8 V to 5.5 V, and the M24C08-F can be accessed either with a supply voltage from 1.7 V to 5.5 V (over the full temperature range) or with an extended supply voltage from 1.6 V to 1.7 V. All these devices operate with a clock frequency of 400 kHz.

Figure 1. Logic diagram

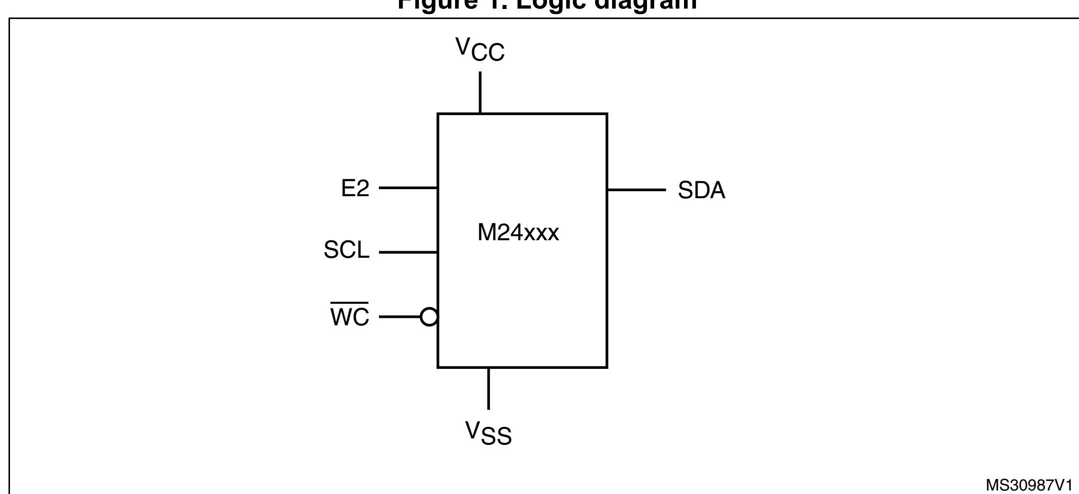
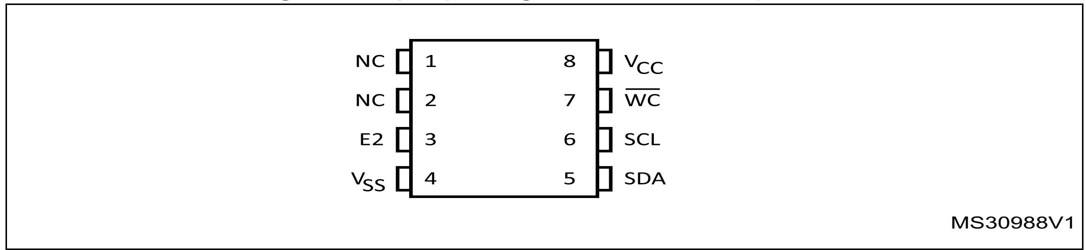


Table 1. Signal names

Signal name	Function	Direction
E2(1)	Chip Enable	Input
SDA	Serial Data	I/O
SCL	Serial Clock	Input
$\overline{WC}$(1)	Write Control	Input
V_{CC}	Supply voltage	-
V_{SS}	Ground	-

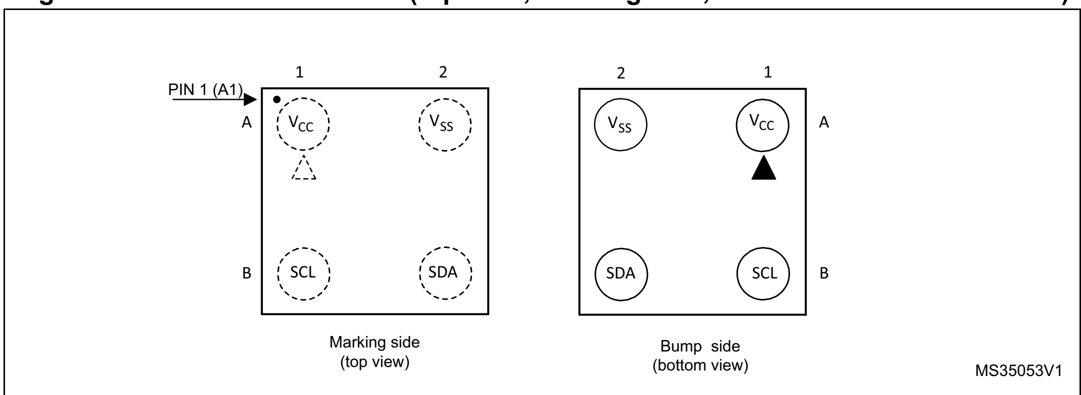
1. Signal not connected in the WLCSP package.

Figure 2. 8-pin package connections, top view



1. NC: not connected.
2. See *Section 9: Package mechanical data* for package dimensions, and how to identify pin 1

Figure 3. WLCSP connections (top view, marking side, with balls on the underside)



1. The E2 and $\overline{WC}$ inputs are not connected to a ball, therefore E2 input is decoded as “0” (see also *Section 2.3: Chip Enable (E2)*) and the device remains always accessible in Write mode (see also *Section 2.4: Write Control ($\overline{WC}$)*).



2 Signal description

2.1 Serial Clock (SCL)

The signal applied on the SCL input is used to strobe the data available on SDA(in) and to output the data on SDA(out).

2.2 Serial Data (SDA)

SDA is an input/output used to transfer data in or data out of the device. SDA(out) is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull-up resistor must be connected from Serial Data (SDA) to V_{CC} (*Figure 12* indicates how to calculate the value of the pull-up resistor).

2.3 Chip Enable (E2)

This input signal is used to set the value that is to be looked for on the bit b3 of the device select code. This input must be tied to V_{CC} or V_{SS}, to establish the device select code as shown in *Figure 4*. When not connected (left floating), this input is read as low (0).

Figure 4. Chip enable inputs connection

2.4 Write Control ($\overline{\text{WC}}$)

This input signal is useful for protecting the entire contents of the memory from inadvertent write operations. Write operations are disabled to the entire memory array when Write Control ($\overline{\text{WC}}$) is driven high. Write operations are enabled when Write Control ($\overline{\text{WC}}$) is either driven low or left floating.

When Write Control ($\overline{\text{WC}}$) is driven high, device select and address bytes are acknowledged, Data bytes are not acknowledged.

2.5 V_{SS} (ground)

V_{SS} is the reference for the V_{CC} supply voltage.

2.6 Supply voltage (V_{CC})

2.6.1 Operating supply voltage (V_{CC})

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see Operating conditions in *Section 8: DC and AC parameters)*. In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a write instruction, until the completion of the internal write cycle (t_W).

2.6.2 Power-up conditions

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage (see Operating conditions in *Section 8: DC and AC parameters)* and the rise time must not vary faster than 1 V/µs.

2.6.3 Device reset

In order to prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included.

At power-up, the device does not respond to any instruction until V_{CC} has reached the internal reset threshold voltage. This threshold is lower than the minimum V_{CC} operating voltage (see Operating conditions in *Section 8: DC and AC parameters*). When V_{CC} passes over the POR threshold, the device is reset and enters the Standby Power mode; however, the device must not be accessed until V_{CC} reaches a valid and stable DC voltage within the specified [V_{CC}(min), V_{CC}(max)] range (see Operating conditions in *Section 8: DC and AC parameters*).

In a similar way, during power-down (continuous decrease in V_{CC}), the device must not be accessed when V_{CC} drops below V_{CC}(min). When V_{CC} drops below the threshold voltage, the device stops responding to any instruction sent to it.

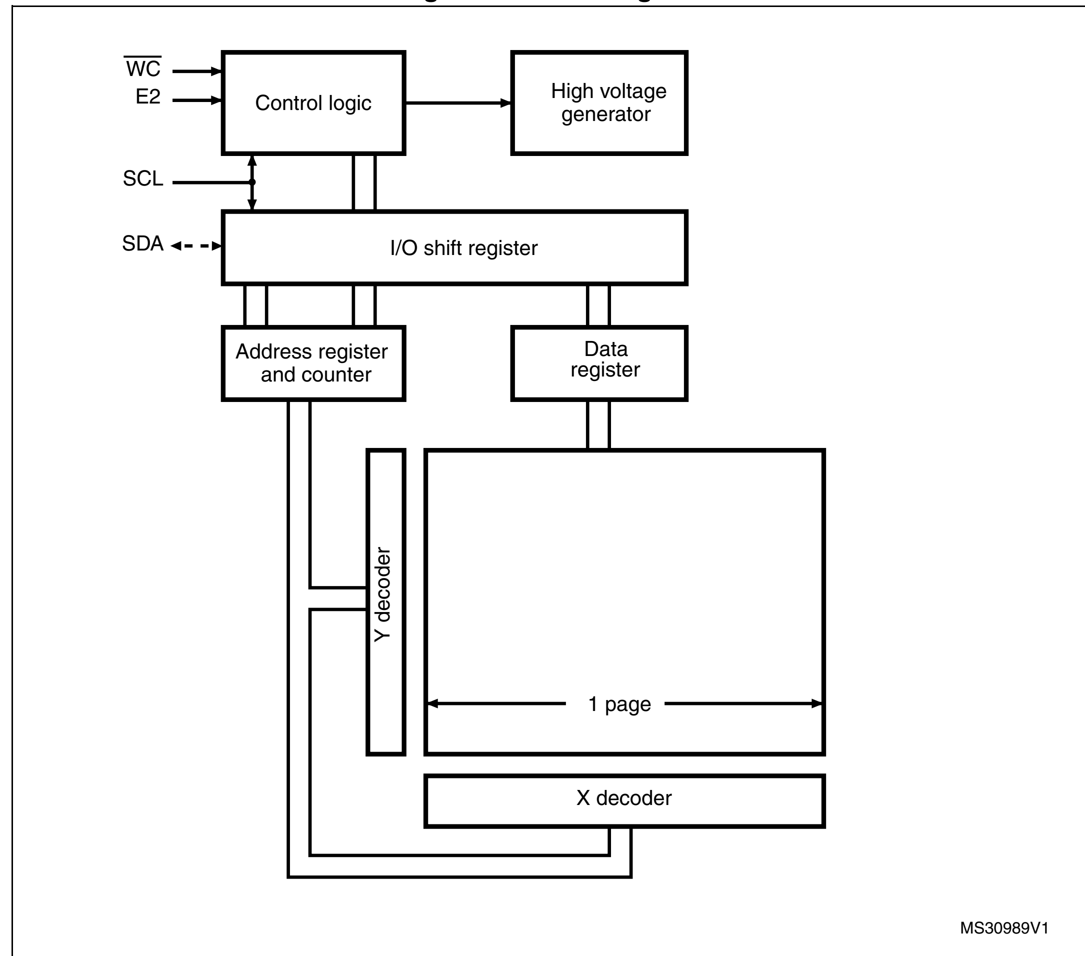
2.6.4 Power-down conditions

During power-down (continuous decrease in V_{CC}), the device must be in the Standby Power mode (mode reached after decoding a Stop condition, assuming that there is no internal write cycle in progress).

3 Memory organization

The memory is organized as shown below.

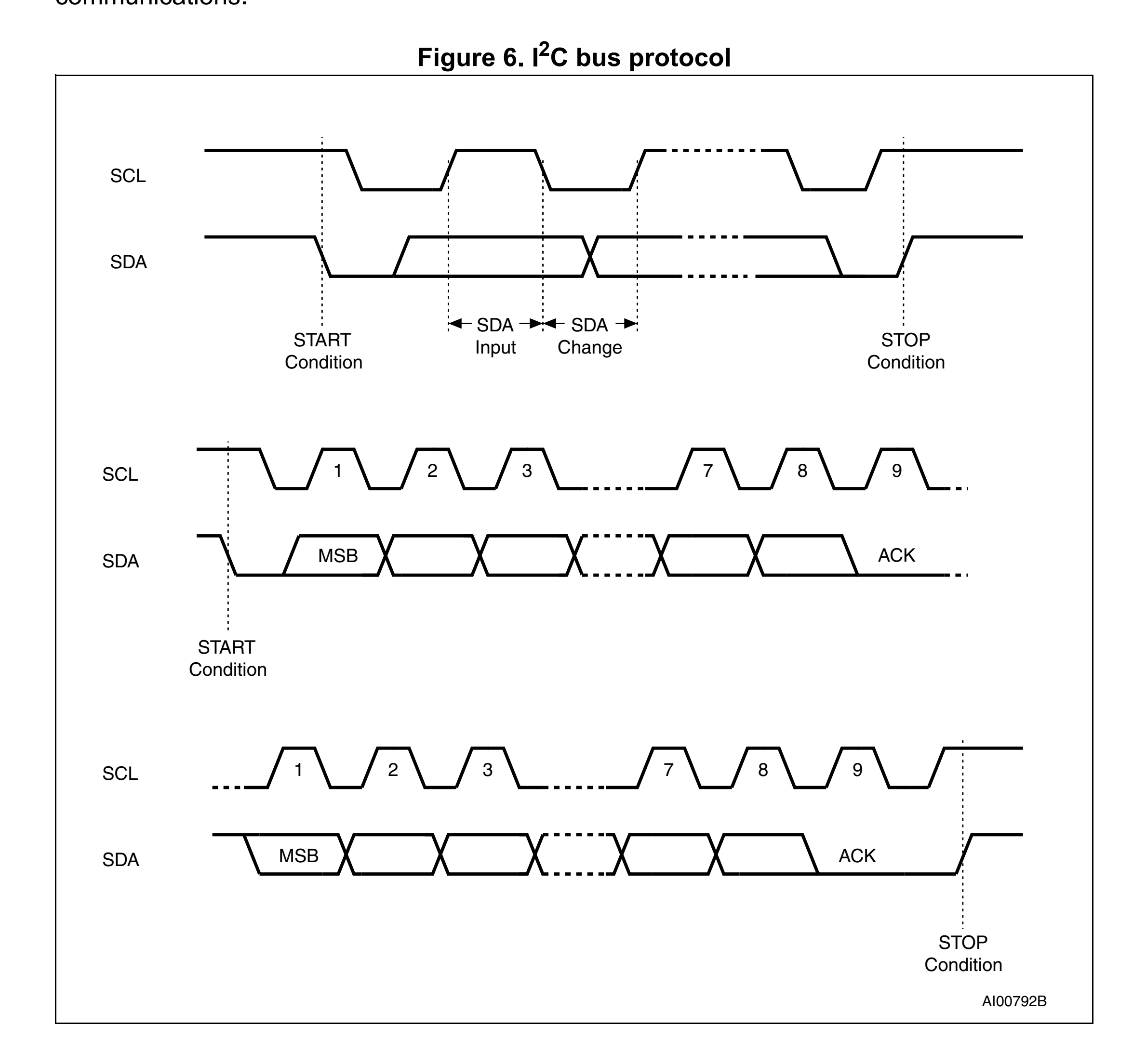
Figure 5. Block diagram



4 Device operation

The device supports the I^2C protocol. This is summarized in *Figure 6*. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The device is always a slave in all communications.

Figure 6. I^2C bus protocol



4.1 Start condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the high state. A Start condition must precede any data transfer instruction. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition.

4.2 Stop condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven high. A Stop condition terminates communication between the device and the bus master. A Read instruction that is followed by NoAck can be followed by a Stop condition to force the device into the Standby mode.

A Stop condition at the end of a Write instruction triggers the internal Write cycle.

4.3 Data input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change *only* when Serial Clock (SCL) is driven low.

4.4 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9^{th} clock pulse period, the receiver pulls Serial Data (SDA) low to acknowledge the receipt of the eight data bits.

4.5 Device addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the device select code, shown in *Table 2* (on Serial Data (SDA), most significant bit first).

Table 2. Device select code

Device type identifier[1]				Chip Enable address			$R\overline{W}$
b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
1	0	1	0	E2	A9	A8	$R\overline{W}$

1. The most significant bit, b7, is sent first.

The 8th bit is the Read/$\overline{\text{Write}}$ bit ($R\overline{W}$). This bit is set to 1 for Read and 0 for Write operations.

If a match occurs on the device select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time. If the device does not match the device select code, it deselects itself from the bus, and goes into Standby mode.



5 Instructions

5.1 Write operations

Following a Start condition the bus master sends a device select code with the R/$\overline{W}$ bit (R$\overline{W}$) reset to 0. The device acknowledges this, as shown in *Figure 7*, and waits for the address byte. The device responds to each address byte with an acknowledge bit, and then waits for the data byte.

Table 3. Address byte

A7	A6	A5	A4	A3	A2	A1	A0

When the bus master generates a Stop condition immediately after a data byte Ack bit (in the "10^{th} bit" time slot), either at the end of a Byte Write or a Page Write, the internal Write cycle t_W is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

After the Stop condition and the successful completion of an internal Write cycle (t_W), the device internal address counter is automatically incremented to point to the next byte after the last modified byte.

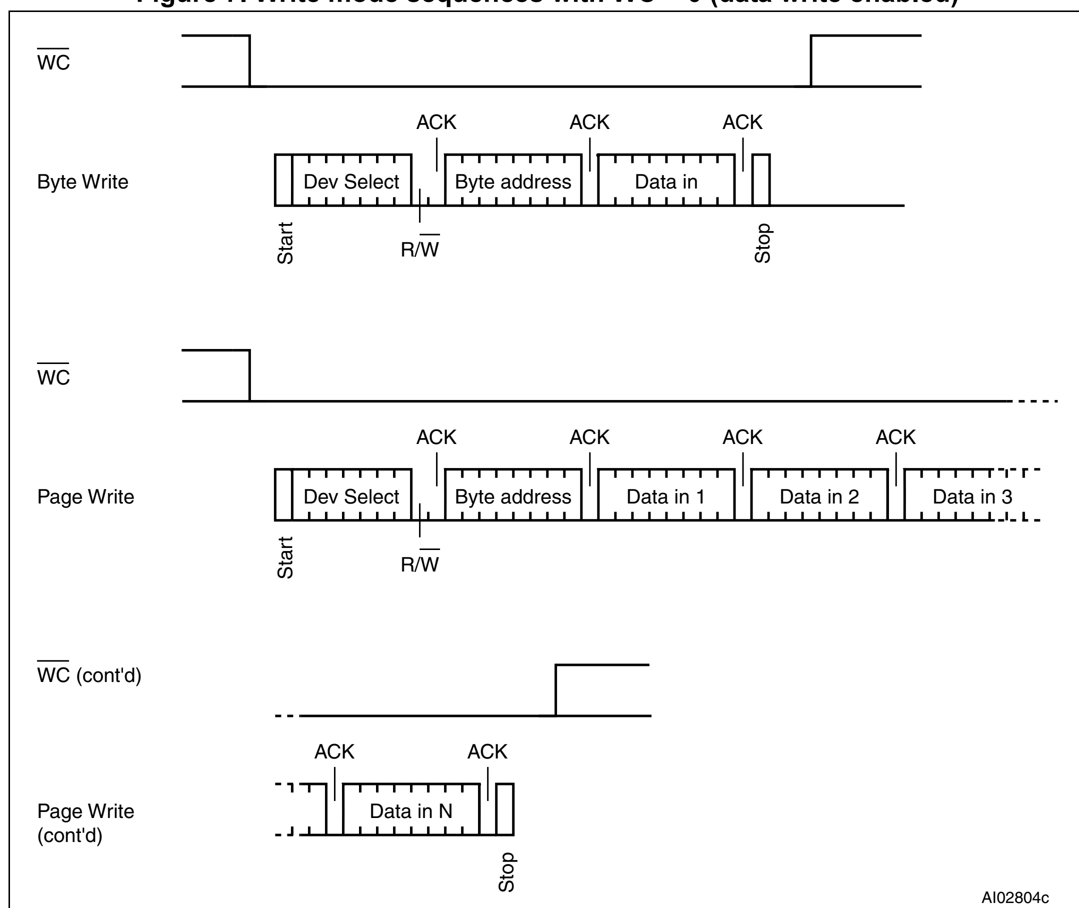
During the internal Write cycle, Serial Data (SDA) is disabled internally, and the device does not respond to any requests.

If the Write Control input (WC) is driven High, the Write instruction is not executed and the accompanying data bytes are *not* acknowledged, as shown in *Figure 8*.

5.1.1 Byte Write

After the device select code and the address byte, the bus master sends one data byte. If the addressed location is Write-protected, by Write Control ($\overline{WC}$) being driven high, the device replies with NoAck, and the location is not modified. If, instead, the addressed location is not Write-protected, the device replies with Ack. The bus master terminates the transfer by generating a Stop condition, as shown in *Figure 7*.

Figure 7. Write mode sequences with $\overline{WC}$ = 0 (data write enabled)



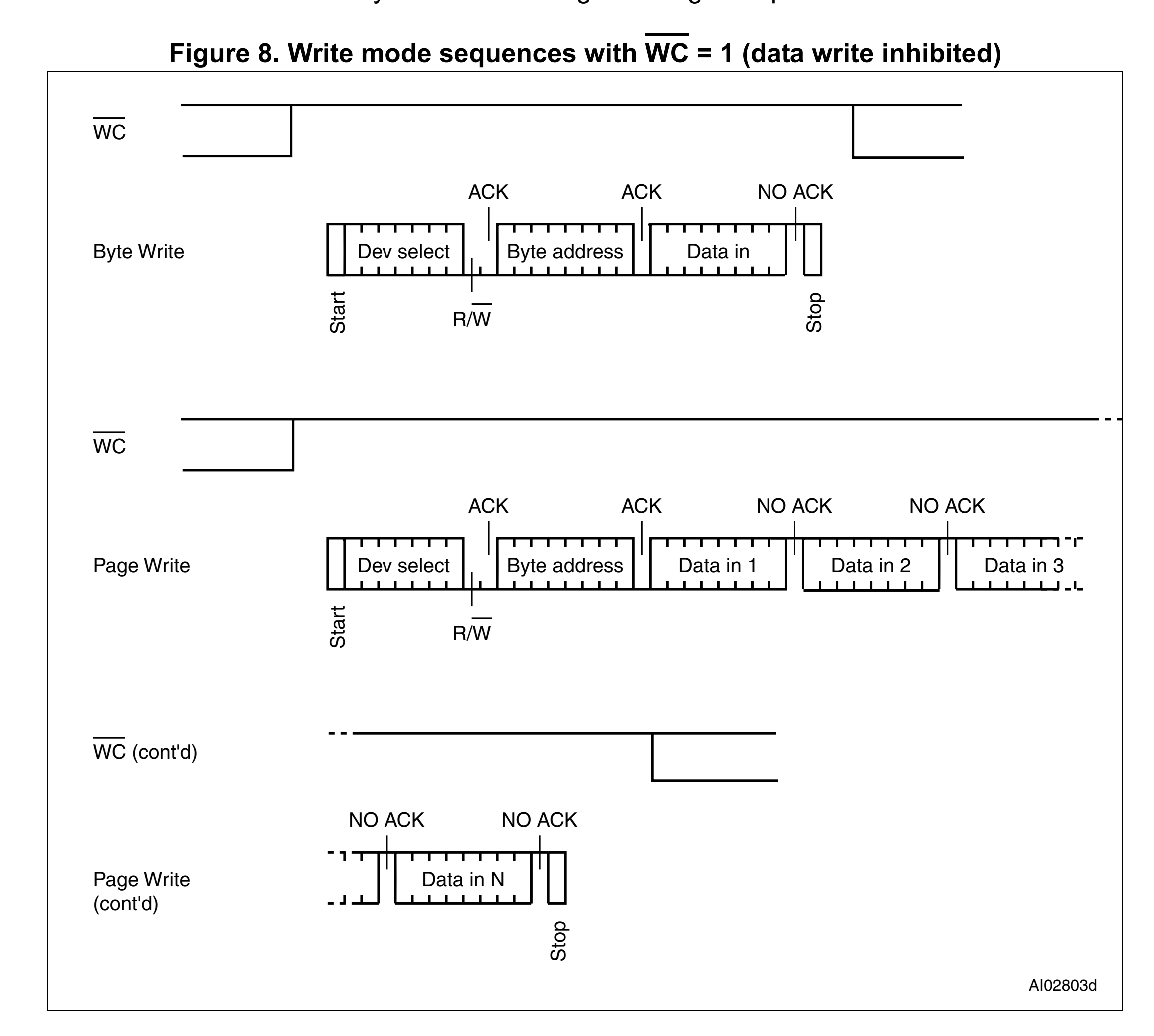
5.1.2 Page Write

The Page Write mode allows up to 16 bytes to be written in a single Write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits, A9/A4, are the same. If more bytes are sent than will fit up to the end of the page, a "roll-over" occurs, i.e. the bytes exceeding the page end are written on the same page, from location 0.

The bus master sends from 1 to 16 bytes of data, each of which is acknowledged by the device if Write Control ($\overline{WC}$) is low. If Write Control ($\overline{WC}$) is high, the contents of the addressed memory location are not modified, and each data byte is followed by a NoAck, as shown in *Figure 8*. After each transferred byte, the internal page address counter is incremented.

The transfer is terminated by the bus master generating a Stop condition.

Figure 8. Write mode sequences with $\overline{WC}$ = 1 (data write inhibited)



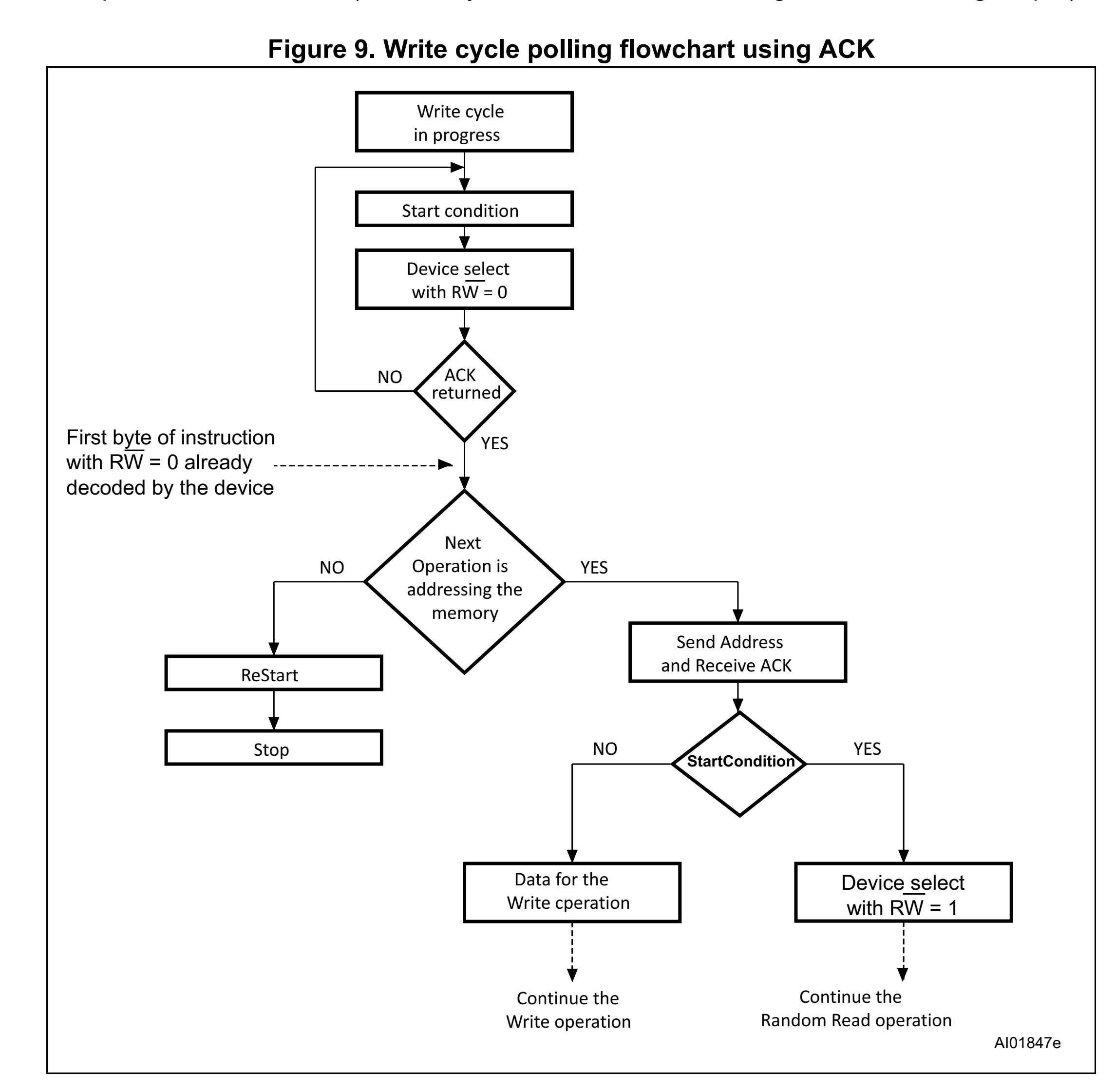
5.1.3 Minimizing Write delays by polling on ACK

The maximum Write time (t_w) is shown in AC characteristics tables in *Section 8: DC and AC parameters*, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in *Figure 9*, is:

- Initial condition: a Write cycle is in progress.
- Step 1: the bus master issues a Start condition followed by a device select code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

Figure 9. Write cycle polling flowchart using ACK



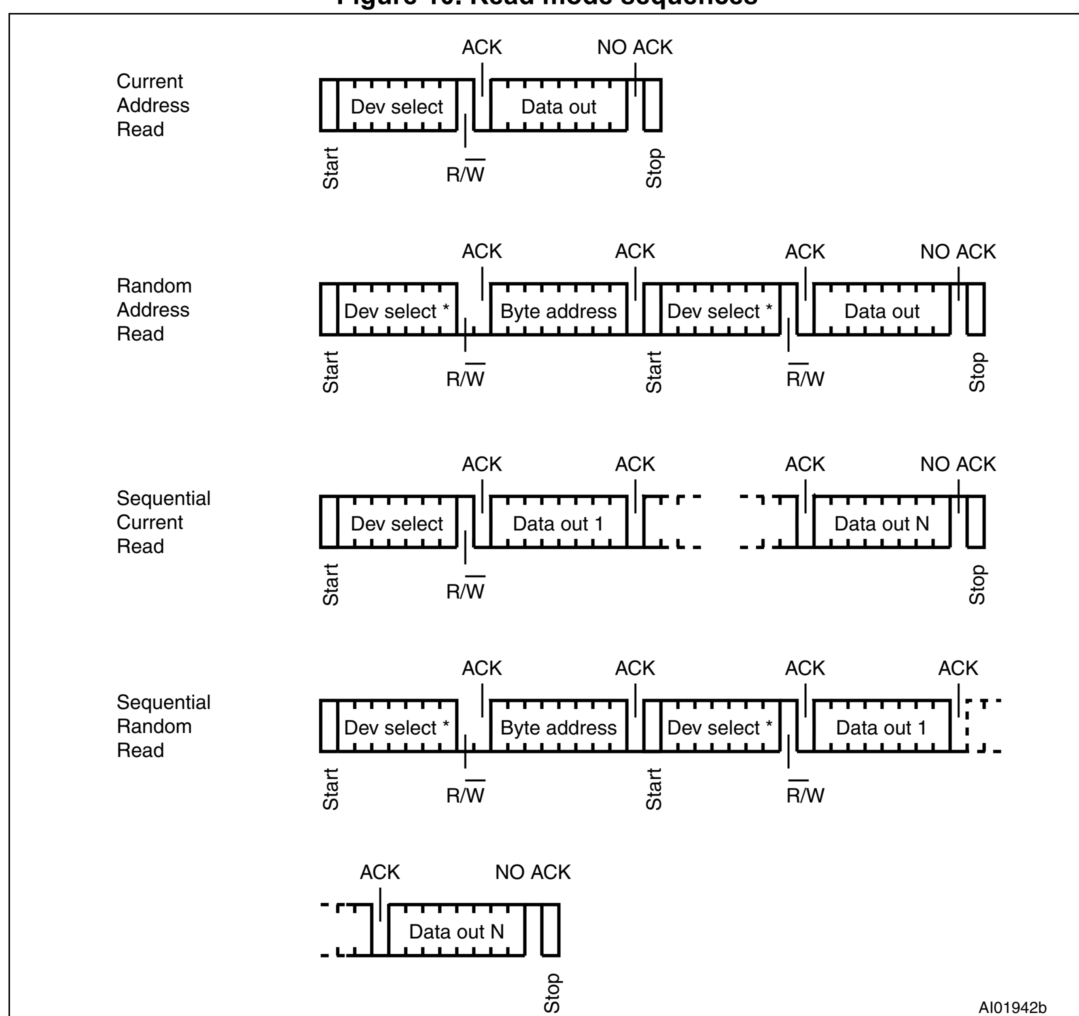
5.2 Read operations

Read operations are performed independently of the state of the Write Control ($\overline{WC}$) signal.

After the successful completion of a Read operation, the device internal address counter is incremented by one, to point to the next byte address.

For the Read instructions, after each byte read (data out), the device waits for an acknowledgment (data in) during the 9th bit time. If the bus master does not acknowledge during this 9th time, the device terminates the data transfer and switches to its Standby mode.

Figure 10. Read mode sequences



5.2.1 Random Address Read

A dummy Write is first performed to load the address into this address counter (as shown in *Figure 10*) but *without* sending a Stop condition. Then, the bus master sends another Start condition, and repeats the device select code, with the R$\overline{W}$ bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must *not* acknowledge the byte, and terminates the transfer with a Stop condition.

5.2.2 Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a device select code with the R/$\overline{W}$ bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in *Figure 10*, *without* acknowledging the byte.

5.2.3 Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master *does* acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must *not* acknowledge the last byte, and *must* generate a Stop condition, as shown in *Figure 10*.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter “rolls-over”, and the device continues to output data from memory address 00h.

6 Initial delivery state

The device is delivered with all the memory array bits set to 1 (each byte contains FFh).

7 Maximum rating

Stressing the device outside the ratings listed in *Table 4* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
	Ambient operating temperature	–40	130	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature during soldering	see note(1)		°C
	PDIP-specific lead temperature during soldering	-	260(2)	°C
I_{OL}	DC output current (SDA = 0)	-	5	mA
V_{IO}	Input or output range	–0.50	6.5	V
V_{CC}	Supply voltage	–0.50	6.5	V
V_{ESD}	Electrostatic pulse (Human Body model)(3)	-	3000(4)	V

1. Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb-free assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions of Hazardous Substances (RoHS directive 2011/65/EU of July 2011).
2. T_{LEAD} max must not be applied for more than 10 s.
3. Positive and negative pulses applied on different combinations of pin connections, according to AEC-Q100-002 (compliant with JEDEC Std JESD22-A114, C1=100 pF, R1=1500 Ω).
4. 4000 V for devices identified by process letters S or G.

8 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device.

Table 5. Operating conditions (voltage range W)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	2.5	5.5	V
T_A	Ambient operating temperature	–40	85	°C
f_C	Operating clock frequency	-	400	kHz

Table 6. Operating conditions (voltage range R)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.8	5.5	V
T_A	Ambient operating temperature	–40	85	°C
f_C	Operating clock frequency	-	400	kHz

Table 7. Operating conditions (voltage range F, for devices identified by process letter T)

Symbol	Parameter	Min.			Max.	Unit
V_{CC}	Supply voltage	1.60	1.65	1.70	5.5	V
T_A	Ambient operating temperature: READ	-40	-40	-40	85	°C
	Ambient operating temperature: WRITE	0	-20	-40	85	
f_C	Operating clock frequency	-	-	-	400	kHz

Table 8. Operating conditions (voltage range F, for all other devices)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.7	5.5	V
T_A	Ambient operating temperature	-20	85	°C
f_C	Operating clock frequency	-	400	kHz

Table 9. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_{bus}	Load capacitance	100		pF
	SCL input rise/fall time, SDA input fall time	-	50	ns
	Input levels	$0.2\ V_{CC}$ to $0.8\ V_{CC}$		V
	Input and output timing reference levels	$0.3\ V_{CC}$ to $0.7\ V_{CC}$		V

Figure 11. AC measurement I/O waveform

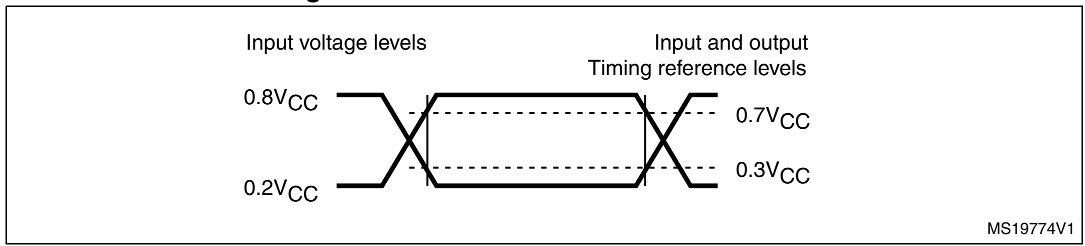


Table 10. Input parameters

Symbol	Parameter[1]	Test condition	Min.	Max.	Unit
C_{IN}	Input capacitance (SDA)	-	-	8	pF
C_{IN}	Input capacitance (other pins)	-	-	6	pF
Z_L	Input impedance ($\overline{WC}$)	$V_{IN} < 0.3\ V_{CC}$	15	70	kΩ
Z_H		$V_{IN} > 0.7\ V_{CC}$	500	-	kΩ

1. Characterized only, not tested in production.

Table 11. Cycling performance

Symbol	Parameter	Test condition[1]	Max.	Unit
Ncycle	Write cycle endurance	$T_A \leq 25$ °C, $V_{CC}(min) < V_{CC} < V_{CC}(max)$	4,000,000	Write cycle
		$T_A = 85$ °C, $V_{CC}(min) < V_{CC} < V_{CC}(max)$	1,200,000	

1. Cycling performance for products identified by process letter T.

Table 12. Memory cell data retention

Parameter	Test condition	Min.	Unit
Data retention[1]	$T_A = 55$ °C	200	Year

1. For products identified by process letter T. The data retention behavior is checked in production, while the 200-year limit is defined from characterization and qualification results.

Table 13. DC characteristics (M24C08-W, device grade 6)

Symbol	Parameter	Test conditions (in addition to those in Table 5 and Table 9)	Min.	Max.	Unit
I_{LI}	Input leakage current (SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC}, device in Standby mode	-	± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}	-	± 2	µA
I_{CC}	Supply current (Read)	V_{CC} = 5.5 V, f_c = 400 kHz	-	1(1)	mA
		V_{CC} = 2.5 V, f_c = 400 kHz	-	1	mA
I_{CC0}	Supply current (Write)	Value overaged over t_W, 2.5 V ≤ V_{CC} ≤ 5.5 V	-	1(2)	mA
I_{CC1}	Standby supply current	Device not selected(3), $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5 V	-	2(4)	µA
		Device not selected(3), $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5.5 V	-	3(4)	µA
V_{IL}	Input low voltage (SCL, SDA, $\overline{WC}$, E2)(5)	-	–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage (SCL, SDA, $\overline{WC}$)	-	0.7 V_{CC}	V_{CC} +1	V
V_{OL}	Output low voltage	I_{OL} = 2.1 mA, V_{CC} = 2.5 V or I_{OL} = 3 mA, V_{CC} = 5.5 V	-	0.4	V

1. 2 mA (at V_{CC} = 5 V) for previous devices identified by process letters G or S.
2. Characterized only (not tested in production) for devices identified by process letter T. $I_{CC0(max)}$ is lower than 0.5 mA when writing data with an ambient temperature greater than 25 °C.
3. The device is not selected after power-up, after a Read instruction (after the Stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a Write instruction).
4. 1 µA for previous devices identified by process letters G or S.
5. E_i inputs should be tied to V_{ss} (see Section 2.3).

Table 14. DC characteristics (M24C08-R, device grade 6)

Symbol	Parameter	Test conditions(1) (in addition to those in *Table 6* and *Table 9*)	Min.	Max.	Unit
I_{LI}	Input leakage current (Ei,SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC}, device in Standby mode	-	± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}	-	± 2	µA
I_{CC}	Supply current (Read)	V_{CC} = 1.8 V, f_c= 400 kHz	-	0.8	mA
I_{CC0}	Supply current (Write)	Value overaged over t_W, $V_{CC} \leq 2.5$ V	-	1(2)	mA
I_{CC1}	Standby supply current	Device not selected(3), $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.8 V	-	1	µA
V_{IL}	Input low voltage (SCL, SDA, $\overline{WC}$)	2.5 V $\leq V_{CC}$	–0.45	0.3 V_{CC}	V
		V_{CC} < 2.5 V	–0.45	0.25 V_{CC}	V
V_{IH}	Input high voltage (SCL, SDA)	V_{CC} < 2.5 V	0.75 V_{CC}	6.5	V
	Input high voltage ($\overline{WC}$)	V_{CC} < 2.5 V	0.75 V_{CC}	V_{CC}+ 0.6	V
V_{OL}	Output low voltage	I_{OL} = 0.7 mA, V_{CC} = 1.8 V	-	0.2	V

1. If the application uses the voltage range R device with 2.5 V $\leq V_{cc} \leq$ 5.5 V and -40 °C < T_A < +85 °C, please refer to *Table 13* instead of this table.
2. Characterized only (not tested in production) for devices identified by process letter T. $I_{CC0(max)}$ is lower than 0.5 mA when writing data with an ambient temperature greater than 25 °C.
3. The device is not selected after power-up, after a Read instruction (after the Stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a Write instruction).

Table 15. DC characteristics (M24C08-F device)

Symbol	Parameter	Test conditions[1] (in addition to those in Table 7, Table 8 and Table 9)	Min.	Max.	Unit
I_{LI}	Input leakage current (Ei,SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC}, device in Standby mode	-	± 2	µA
I_{LO}	Output leakage current	$V_{OUT} = V_{SS}$ or V_{CC}, SDA in Hi-Z	-	± 2	µA
I_{CC}	Supply current (Read)	V_{CC} = 1.6 V[2] or 1.7 V, f_c= 400 kHz	-	0.8	mA
I_{CC0}	Supply current (Write)	Value overaged over t_W, $V_{CC} \leq 2.5$ V	-	1[3]	mA
I_{CC1}	Standby supply current	Device not selected[4], $V_{IN} = V_{SS}$ or V_{CC}, $V_{CC} \leq 1.8$ V	-	1	µA
V_{IL}	Input low voltage (SCL, SDA, $\overline{WC}$)	2.5 V ≤ V_{CC}	–0.45	0.3 V_{CC}	V
		V_{CC} < 2.5 V	–0.45	0.25 V_{CC}	V
V_{IH}	Input high voltage (SCL, SDA)	V_{CC} < 2.5 V	0.75 V_{CC}	6.5	V
	Input high voltage ($\overline{WC}$)	V_{CC} < 2.5 V	0.75 V_{CC}	V_{CC}+0.6	V
V_{OL}	Output low voltage	I_{OL} = 0.7 mA, $V_{CC} \leq 1.8$ V	-	0.2	V

1. If the application uses the voltage range F device with 2.5 V ≤ V_{cc} ≤ 5.5 V, please refer to Table 13 instead of this table.
2. 1.6 V for devices identified by process letter T.
3. Characterized only (not tested in production) for devices identified by process letter T. $I_{CC0(max)}$ is lower than 0.5 mA when writing data with an ambient temperature greater than 25 °C.
4. The device is not selected after power-up, after a Read instruction (after the Stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a Write instruction).

Table 16. 400 kHz AC characteristics

Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCL}	Clock frequency	-	400	kHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	600	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	1300	-	ns
t_{QL1QL2}(1)	t_F	SDA (out) fall time	20(2)	300	ns
t_{XH1XH2}	t_R	Input signal rise time	(3)	(3)	ns
t_{XL1XL2}	t_F	Input signal fall time	(3)	(3)	ns
t_{DXCH}	$t_{SU:DAT}$	Data in set up time	100	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	ns
t_{CLQX}(4)	t_{DH}	Data out hold time	100	-	ns
t_{CLQV}(5)	t_{AA}	Clock low to next data valid (access time)	-	900	ns
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	600	-	ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	600	-	ns
t_{CHDH}	$t_{SU:STO}$	Stop condition set up time	600	-	ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	1300	-	ns
t_W	t_{WR}	Write time	-	5	ms
t_{NS}(1)		Pulse width ignored (input filter on SCL and SDA) - single glitch	-	100	ns

1. Characterized only, not tested in production.
2. With C_L = 10 pF.
3. There is no min. or max. values for the input signal rise and fall times. It is however recommended by the I²C specification that the input signal rise and fall times be more than 20 ns and less than 300 ns when f_C < 400 kHz.
4. The min value for t_{CLQX} (Data out hold time) of the M24xxx devices offers a safe timing to bridge the undefined region of the falling edge SCL.
5. t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either 0.3 V_{CC} or 0.7 V_{CC}, assuming that $R_{bus} \times C_{bus}$ time constant is within the values specified in *Figure 12*.

Table 17. 100 kHz AC characteristics (I^2C Standard mode)(1)

Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCL}	Clock frequency	-	100	kHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	4	-	µs
t_{CLCH}	t_{LOW}	Clock pulse width low	4.7	-	µs
t_{XH1XH2}	t_R	Input signal rise time	-	1	µs
t_{XL1XL2}	t_F	Input signal fall time	-	300	ns
t_{QL1QL2}(2)	t_F	SDA fall time	-	300	ns
t_{DXCH}	$t_{SU:DAT}$	Data in setup time	250	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	ns
t_{CLQX}(3)	t_{DH}	Data out hold time	200	-	ns
t_{CLQV}(4)	t_{AA}	Clock low to next data valid (access time)	-	3450	ns
t_{CHDL}(5)	$t_{SU:STA}$	Start condition setup time	4.7	-	µs
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	4	-	µs
t_{CHDH}	$t_{SU:STO}$	Stop condition setup time	4	-	µs
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	4.7	-	µs
t_W	t_{WR}	Write time	-	5	ms
t_{NS}(2)		Pulse width ignored (input filter on SCL and SDA), single glitch	-	100	ns

1. Values recommended by the I^2C bus Standard-mode specification for a robust design of the I^2C bus application. Note that the M24xxx devices decode correctly faster timings as specified in *Table 16: 400 kHz AC characteristics*.
2. Characterized only.
3. To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
4. t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either 0.3 V_{CC} or 0.7 V_{CC}, assuming that Rbus × Cbus time constant is within the values specified in *Figure 12*.
5. For a reStart condition, or following a Write cycle.

Figure 12. Maximum R_{bus} value versus bus parasitic capacitance (C_{bus}) for an I^2C bus at maximum frequency f_C = 400 kHz

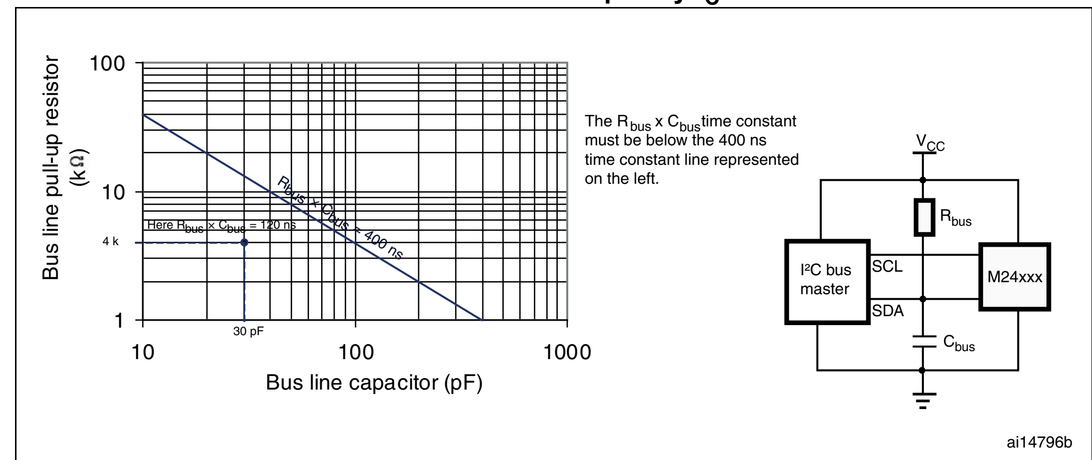
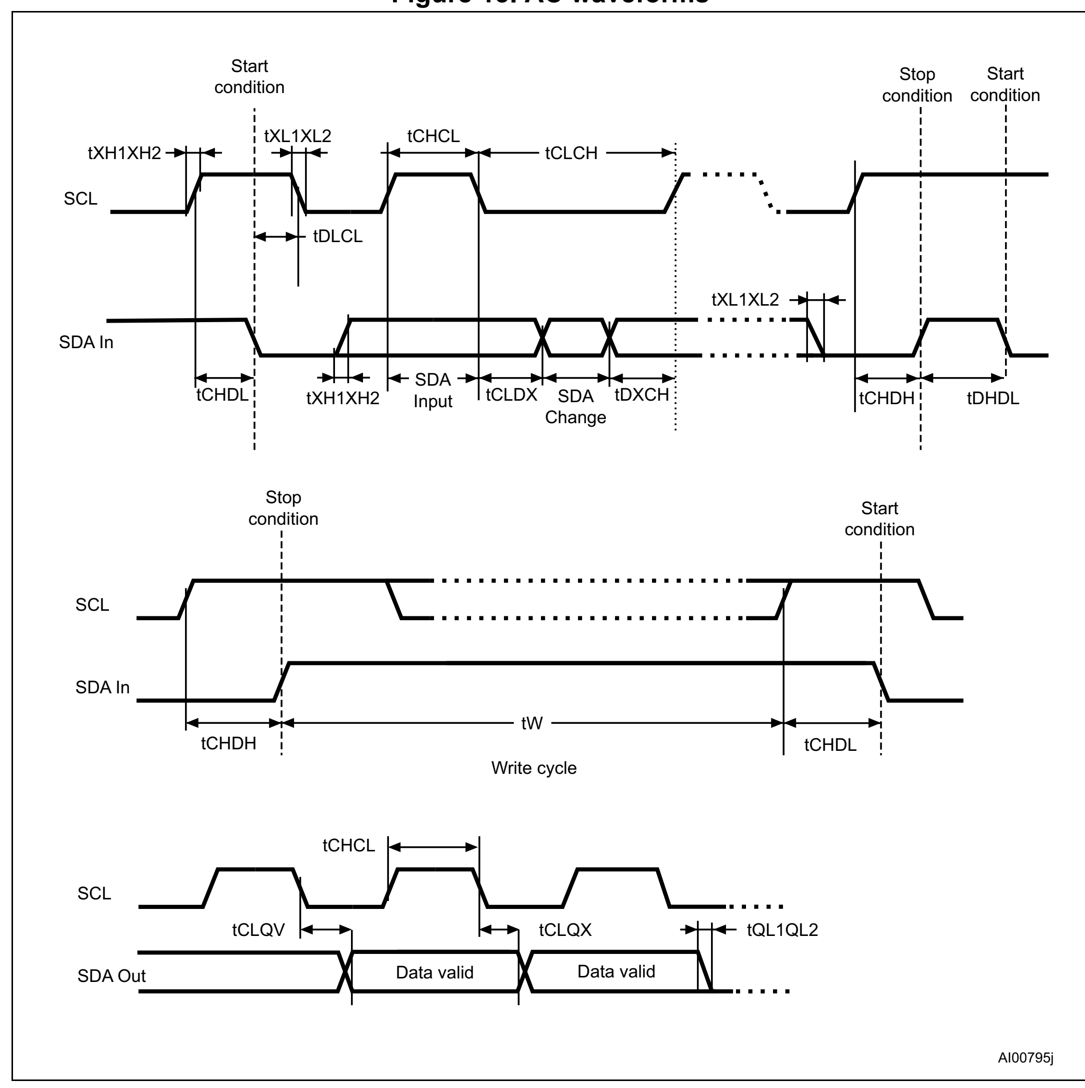


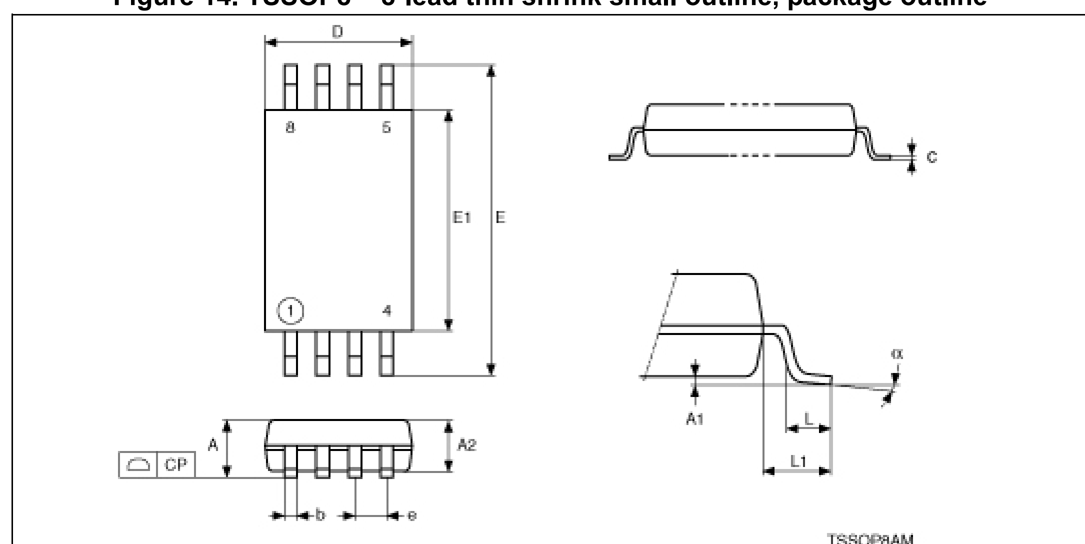
Figure 13. AC waveforms



9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 14. TSSOP8 – 8-lead thin shrink small outline, package outline



1. Drawing is not to scale.

Table 18. TSSOP8 – 8-lead thin shrink small outline, package mechanical data

Symbol	millimeters			inches(1)		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	–	–	1.200	–	–	0.0472
A1	–	0.050	0.150	–	0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b	–	0.190	0.300	–	0.0075	0.0118
c	–	0.090	0.200	–	0.0035	0.0079
CP	–	–	0.100	–	–	0.0039
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	–	–	0.0256	–	–
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000	–	–	0.0394	–	–
α	–	0°	8°	–	0°	8°

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 15. SO8N – 8-lead plastic small outline, 150 mils body width, package outline

1. Drawing is not to scale.

Table 19. SO8N – 8-lead plastic small outline, 150 mils body width, package data

Symbol	millimeters			inches (1)		
	Typ	Min	Max	Typ	Min	Max
A	–	–	1.750	–	–	0.0689
A1	–	0.100	0.250	–	0.0039	0.0098
A2	–	1.250	–	–	0.0492	–
b	–	0.280	0.480	–	0.0110	0.0189
c	–	0.170	0.230	–	0.0067	0.0091
ccc	–	–	0.100	–	–	0.0039
D	4.900	4.800	5.000	0.1929	0.1890	0.1969
E	6.000	5.800	6.200	0.2362	0.2283	0.2441
E1	3.900	3.800	4.000	0.1535	0.1496	0.1575
e	1.270	–	–	0.0500	–	–
h	–	0.250	0.500	–	0.0098	0.0197
k	–	0°	8°	–	0°	8°
L	–	0.400	1.270	–	0.0157	0.0500
L1	1.040	–	–	0.0409	–	–

1. Values in inches are converted from mm and rounded to four decimal digits.



Figure 16. PDIP8 – 8-pin plastic DIP, 0.25 mm lead frame, package outline

1. Drawing is not to scale.
2. Not recommended for new designs.

Table 20. PDIP8 – 8-pin plastic DIP, 0.25 mm lead frame, package mechanical data

Symbol	millimeters			inches[1]		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	–	–	5.33	–	–	0.2098
A1	–	0.38	–	–	0.0150	–
A2	3.30	2.92	4.95	0.1299	0.1150	0.1949
b	0.46	0.36	0.56	0.0181	0.0142	0.0220
b2	1.52	1.14	1.78	0.0598	0.0449	0.0701
c	0.25	0.20	0.36	0.0098	0.0079	0.0142
D	9.27	9.02	10.16	0.3650	0.3551	0.4000
E	7.87	7.62	8.26	0.3098	0.3000	0.3252
E1	6.35	6.10	7.11	0.2500	0.2402	0.2799
e	2.54	–	–	0.1000	–	–
eA	7.62	–	–	0.3000	–	–
eB	–	–	10.92	–	–	0.4299
L	3.30	2.92	3.81	0.1299	0.1150	0.1500

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 17. UFDFPN8 (MLP8) – package outline (UFDFPN: Ultra thin Fine pitch Dual Flat Package, No lead)

1. Drawing is not to scale.
2. The central pad (area E2 by D2 in the above illustration) is internally pulled to V_{SS}. It must not be connected to any other voltage or signal line on the PCB, for example during the soldering process.

Table 21. UFDFPN8 (MLP8) – package dimensions (UFDFPN: Ultra thin Fine pitch Dual Flat Package, No lead)

Symbol	millimeters			inches(1)		
	Typ	Min	Max	Typ	Min	Max
A	0.550	0.450	0.600	0.0217	0.0177	0.0236
A1	0.020	0.000	0.050	0.0008	0.0000	0.0020
b	0.250	0.200	0.300	0.0098	0.0079	0.0118
D	2.000	1.900	2.100	0.0787	0.0748	0.0827
D2 (rev MC)	–	1.200	1.600	–	0.0472	0.0630
E	3.000	2.900	3.100	0.1181	0.1142	0.1220
E2 (rev MC)	–	1.200	1.600	–	0.0472	0.0630
e	0.500	–	–	0.0197	–	–
K (rev MC)	–	0.300	–	–	0.0118	–
L	–	0.300	0.500	–	0.0118	0.0197
L1	–	–	0.150	–	–	0.0059
L3	–	0.300	–	–	0.0118	–
eee(2)	–	0.080	–	–	0.0031	–

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Applied for exposed die paddle and terminals. Exclude embedding part of exposed die paddle from measuring.

Figure 18. M24C08-FCT6TP/T package outline

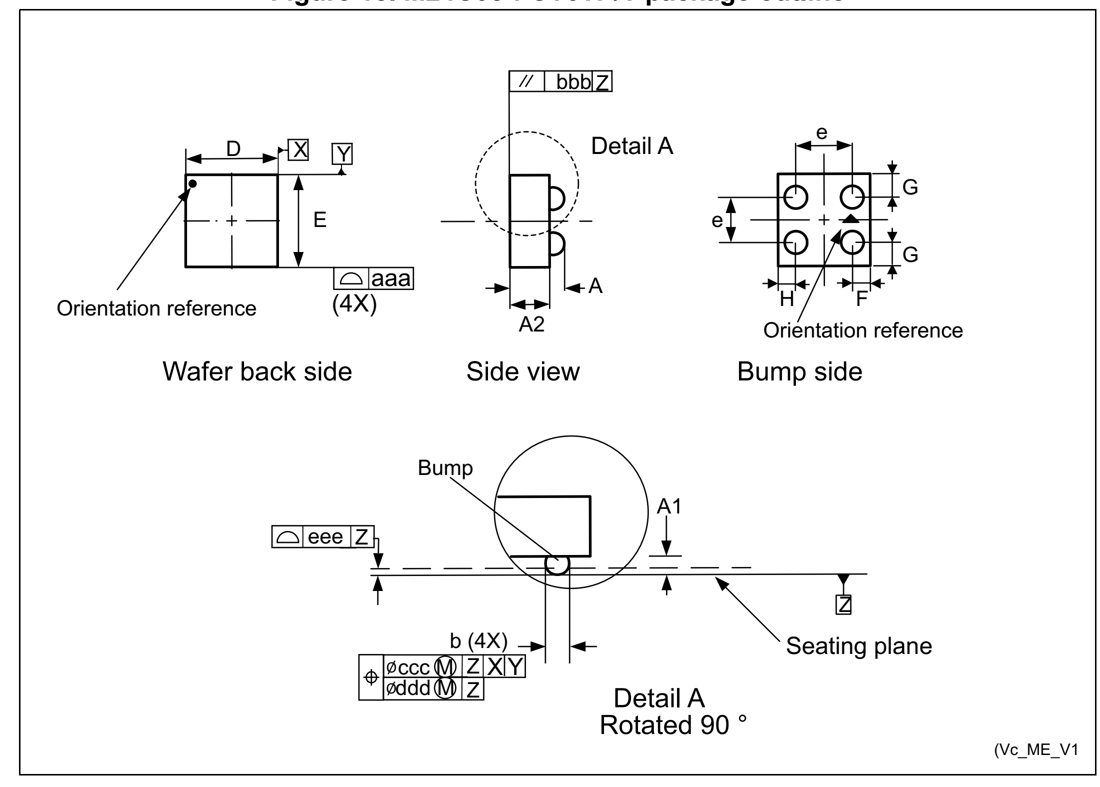
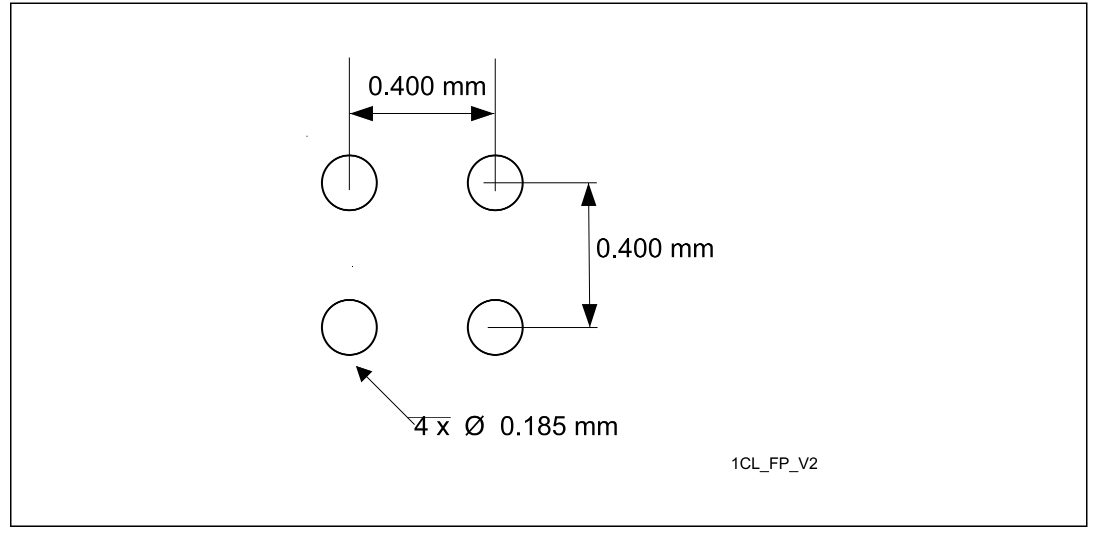




Table 22. M24C08-FCT6TP/T package data

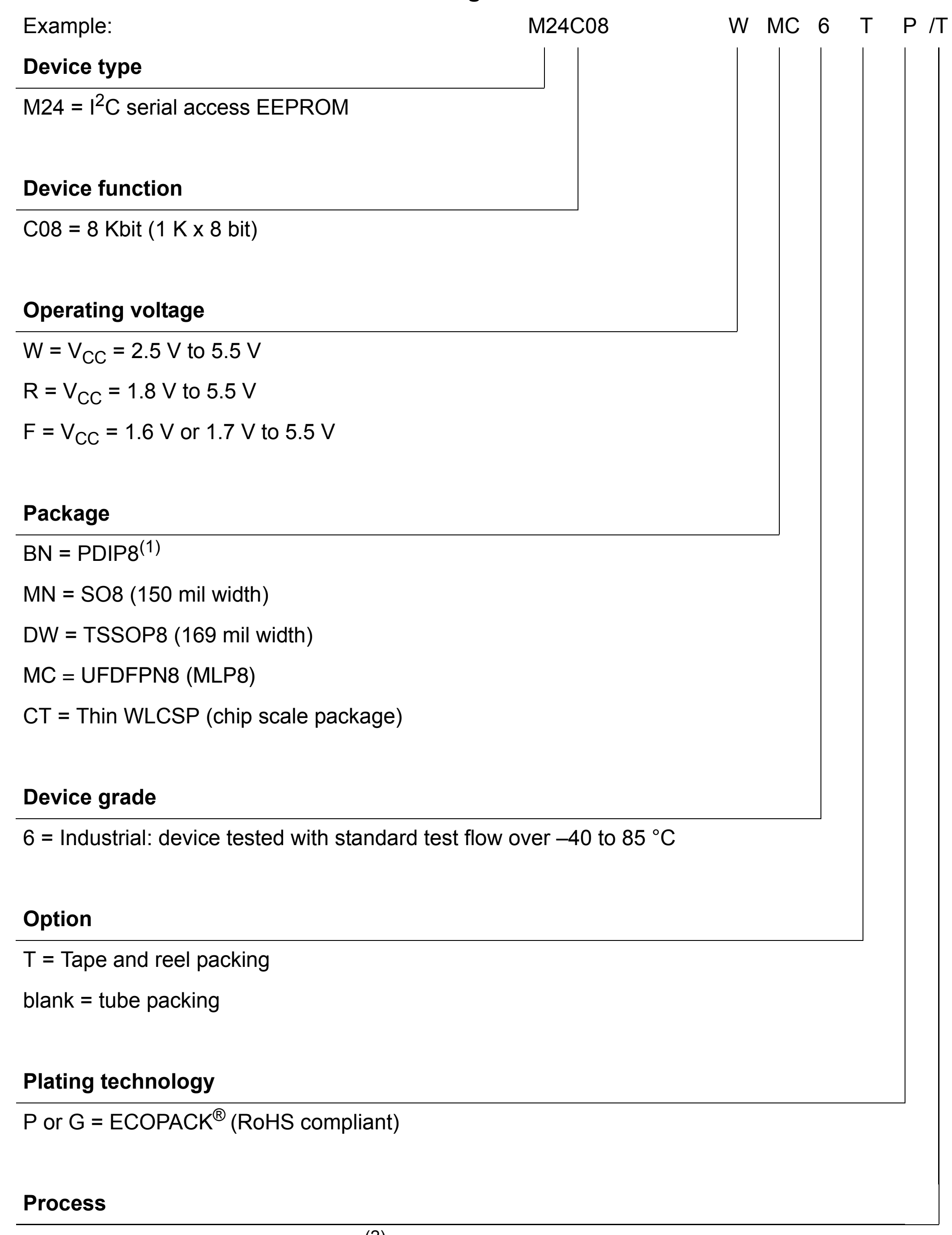
Symbol	millimeters			inches		
	TYP	MIN	MAX	TYP	MIN	MAX
A	0.295	0.270	0.330	0.0116	0.0106	0.0130
A1	0.095	-	-	0.0037	-	-
A2	0.200	-	-	0.0079	-	-
Ø b	0.185	-	-	0.0073	-	-
D	0.685	-	0.705	0.0270	-	0.0278
E	0.695	-	0.715	0.0274	-	0.0281
e	0.400	-	-	0.0157	-	-
F	0.142	-	-	0.0056	-	-
G	0.148	-	-	0.0058	-	-
H	0.143	-	-	0.0056	-	-
N	4					
aaaa	0.110	-	-	0.0043	-	-
bbbb	0.110	-	-	0.0043	-	-
cccc	0.110	-	-	0.0043	-	-
dddd	0.060	-	-	0.0024	-	-
eeee	0.060	-	-	0.0024	-	-

Figure 19. WLCSP 4-bump wafer-level chip-scale package recommended land pattern



10 Part numbering

Table 23. Ordering information scheme



1. Not recommended for new designs.
2. The process letter is required only for the WLCSP device

11 Revision history

Table 24. Document revision history

Date	Revision	Changes
17-Dec-2012	1	New single product M24C08 datasheet resulting from splitting the previous datasheet M24C08-x M24C04-x M24C02-x M24C01-x (revision 18) into separate datasheets.
25-Sep-2013	2	Added: – *Table 11: Cycling performance* – *Table 7: Operating conditions (voltage range F, for devices identified by process letter T)* and *Table 8: Operating conditions (voltage range F, for all other devices)*. Updated: – *Features*: supply voltage, write cycles and data retention – *Section 1: Description* – *Table 4: Absolute maximum ratings*, *Table 12: Memory cell data retention*, *Table 13: DC characteristics (M24C08-W, device grade 6)*, *Table 14: DC characteristics (M24C08-R, device grade 6)*, *Table 15: DC characteristics (M24C08-F device)*, *Table 23: Ordering information scheme* – *Figure 13: AC waveforms* Renamed *Figure 17* and *Table 21*. Replaced “5 bump” by “M24C08-FCT5TP/S” in WLCSP package description.
17-Dec-2013	3	Added *Figure 4: Chip enable inputs connection* Updated: – *Table 13: DC characteristics (M24C08-W, device grade 6)* – *Table 14: DC characteristics (M24C08-R, device grade 6)* – *Table 15: DC characteristics (M24C08-F device)* – *Figure 13: AC waveforms* – *Table 23: Ordering information scheme*
04-Jun-2014	4	Updated: Package on cover page added note (1) on *Table 1: Signal names*. Updated note (1) and picture, deleted Caution note on *Figure 3*. Updated note (4) on *Table 4*. Corrected wrong Symbol name t_{DXCX} in t_{DXCH} in *Table 16*. Updated *Figure 18: M24C08-FCT6TP/T package outline* and *Table 22: M24C08-FCT6TP/T package data*. Added “Process” row specification in *Table 23: Ordering information scheme*. Added *Figure 19*



